Shri Vaishnav Vidyapeeth Vishwavidyalaya
Shri Vaishnav Institute of Technology and Science
Choice Based Credit System (CBCS) Scheme in the light of NEP-2020
M.Tech. (VLSI Design)

SEMESTER-I (2025-2027)

S. No.	COURSE CODE	COURSE NAME	TEACHING SCHEME/WEEK			CREDITS	EXAMINATION SCHEME					TOTAL MARKS
							THEORY			PRACTICAL		
			L	T	P		End Sem Unversity Exam (60%)	Two Term Exam (20%)	Teachers Assess-ment* (20%)	End Sem Unversity Exam (60%)	Teachers Assess-ment* (40%)	
1	MBAI301C	Advanced Human Values and Professional Ethics	3	0	0	3	60	20	20	0	0	100
2	MTMAN101	Advanced Mathematics	3	0	0	3	60	20	20	0	0	100
3	MTVD101	FPGA Based System Design	3	0	2	4	60	20	20	30	20	150
4	MTVD102	CMOS VLSI Design	3	0	2	4	60	20	20	30	20	150
5	-	Elective I	3	0	0	3	60	20	20	0	0	100
6	MTVD104	Design Verification Lab	0	0	4	2	0	0	0	30	20	50
7	MTVD105	Comprehensive Viva	0	0	2	1	0	0	0	30	20	50
TOTAL			**15**	**0**	**5**	**20**	**300**	**100**	**100**	**120**	**80**	**700**

Legends: L - Lecture ; T - Tutorial/Teacher Guided Student Activity ; P - Practical

***Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.**

Elective I		
S. No.	**Course Code**	**Course Name**
1	MTVD113	VLSI Technology
2	MTVD123	Microelectronics: Devices to Circuits
3	MTVD133	RF IC Design

26/7/25

Chairperson
Board of Studies
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore

Chairperson
Faculty of Studies
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore

Controller of Examinations
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore

Registrar
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore

26.7.25

Vice Chancellor
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore